1. A method of forming a semiconductor device, comprising:

forming a first contact stud and a second contact stud, each said contact stud comprising silicon and being connected to a respective active area of a semiconductor substrate;

forming a first silicide cap on top of said first contact stud and a second silicide cap on top of said second contact stud;

forming an interconnect line above said first contact stud and in contact with said first silicide cap, and at least in partial contact with said second silicide cap; and

isolating said interconnect line from said second contact stud by selectively removing at least a portion of said second silicide cap and providing an insulator between said interconnect line and said second contact stud.

2. The method of claim 1, wherein said first and second contact studs are formed by selective deposition of epitaxial silicon.

3. The method of claim 2, wherein said isolating comprises:

forming an insulating layer over and around said interconnect line;

forming a contact hole through said insulating layer to remove at least a portion of said second silicide cap; and

forming an insulating sidewall inside said contact hole which insulates said second contact stud from said interconnect line.

4. The method of claim 3, further comprising forming a conductive plug within said contact hole and said insulating sidewalls and in electrical contact with said second contact stud.

5. The method of claim 4, wherein said conductive plug is formed of polysilicon.

6. The method of claim 4, wherein said conductive plug is formed of selectively deposited epitaxial silicon.

7. The method of claim 2, wherein said first and second contact studs are formed simultaneously.

8. The method of claim 2, wherein said interconnect line is a bit line of a memory cell.

9. The method of claim 2, further comprising forming a capacitor in electrical contact with said second contact stud.

10. The method of claim 9, comprising forming a bottom electrode of said capacitor simultaneously with the forming of a conductive plug electrically connected to said second contact stud.

11. The method of claim 2, wherein said selective removing of said second silicide cap includes wet etching.

12. The method of claim 3, wherein said insulating sidewall is formed of a layer of at least one of SiO_2 and Si_3N_4.

13. The method of claim 4, wherein said conductive plug comprises a metal-based material.

14. The method of claim 13, wherein said metal-based material is formed of one or more materials selected from the group consisting of W, TiN, Pt, Ru, Al, alloys of the preceding, oxides of the preceding, carbides of the preceding, borides of the preceding, and combinations of the foregoing.

15. The method of claim 13, wherein said metal-based material is formed of one or more materials selected from the group consisting of a metal of

Groups IVB, VB, VIB, VIII, IB, IIB, or IIIA of the Periodic Table, alloys of the preceding, oxides of the preceding, carbides of the preceding, borides of the preceding, and combinations of the foregoing.

16. The method of claim 2, wherein said semiconductor device is a memory device.

17. A method of forming at least a portion of a DRAM cell array, said method comprising:

forming at least one transistor gate and associated source and drain regions on a semiconductor substrate;

selectively depositing epitaxial silicon over said source and drain regions to form a first contact stud and a second contact stud;

forming a first silicide cap on top of said first contact stud and a second silicide cap on top of said second contact stud;

forming an interconnect line above said first contact stud and in contact with said first silicide cap, and at least in partial contact with said second silicide cap; and

selectively removing at least a portion of said second silicide cap where in contact with said interconnect line.

18. A method as in claim 17, further comprising forming an insulating sidewall inside a contact hole to said second contact stud, wherein said contact hole is through an insulating layer which is formed over and around said interconnect line.

19. A method as in claim 18, further comprising forming a conductive plug within said contact hole and said insulating sidewall and in electrical contact with said second contact stud.

20. The method of claim 19, wherein said conductive plug is formed by selective deposition of epitaxial silicon.

21. The method of claim 17, wherein said first and second contact studs are formed simultaneously.

22. The method of claim 17, wherein said first and second silicide caps are formed utilizing a selective deposition method.

23. The method of claim 17, further comprising forming a capacitor in electrical contact with said second contact stud.

24. The method of claim 23, comprising forming a bottom electrode of said capacitor simultaneously with the forming of a conductive plug electrically connected to said second contact stud.

25. The method of claim 17, wherein said interconnect line is a bit line.

26. The method of claim 17, wherein said selective removing of at least a portion of said second silicide cap includes wet etching.

27. The method of claim 18, wherein said insulating sidewall is formed by depositing a thin dielectric layer within said contact hole and etching said thin dielectric layer.

28. The method of claim 27, wherein said thin dielectric layer comprises a material selected from at least one of SiO_2 and Si_3N_4.

29. The method of claim 19, wherein said conductive plug is formed of a material selected from the group consisting of polysilicon and a metal-based material.

30. The method of claim 29, wherein said metal-based material is formed of one or more materials selected from the group consisting of W, TiN, Pt,

Ru, and Al, alloys of the preceding, oxides of the preceding, carbides of the preceding, borides of the preceding, and combinations of the foregoing.

31. The method of claim 29, wherein said metal-based material is formed of one or more materials selected from the group consisting of a metal selected from Groups IVB, VB, VIB, VIII, IB, IIB, or IIIA of the Periodic Table, alloys of the preceding, oxides of the preceding, carbides of the preceding, borides of the preceding, and combinations of the foregoing.

32. A method of forming a semiconductor device, comprising:

forming a least one gate structure and associated active areas on a semiconductor substrate;

forming a first insulating layer over said gate structure and said substrate;

etching at least a first and a second contact hole through said first insulating layer to respective one of said active area;

selectively depositing epitaxial silicon to form at least a first and a second contact stud within said first and second contact holes, respectively;

forming at least a first and a second silicide cap on said first and second contact studs, respectively;

forming at least one interconnect line over said contact studs and silicide caps, wherein said interconnect line is in contact with said first silicide cap and at least in partial contact with said second silicide cap;

forming a second insulating layer over and around said interconnect line;

etching at least one third contact hole in said second insulating layer to said second silicide cap;

removing at least a portion of said second silicide cap within said third contact hole where in contact with said interconnect line;

forming a third insulating layer at least within said third contact hole and between said interconnect line and said second contact stud;

etching said third insulating layer to said second contact stud to form insulating sidewalls within said third contact hole; and

forming a conductive plug in contact with said second contact stud and within said insulating sidewalls.

33. The method of claim 32, wherein said first and second contact studs are formed simultaneously.

34. The method of claim 32, comprising forming said conductive plug by selective deposition of epitaxial silicon.

35. The method of claim 32, further comprising forming a capacitor in electrical contact with said second contact stud, and wherein said at least one interconnect line is a bit line of said memory device which is connected to said respective one of said active areas by said first contact stud.

36. The method of claim 32, comprising forming a bottom electrode of said capacitor simultaneously with forming said conductive plug.

37. A method of isolating an interconnect line from a partially underlying contact of a DRAM memory cell, said method comprising:

selectively depositing epitaxial silicon to form a first contact stud over a first active area on a semiconductor substrate and a second contact stud over a second active area on said semiconductor substrate;

forming an interconnect line over said first contact stud and at least in partial contact with said second contact stud;

etching a contact hole to said second contact stud, through an insulating layer formed over and around said interconnect line, and selectively

etching a portion of said second contact stud to remove any direct electrical contact with said interconnect line;

forming insulating sidewalls in said contact hole to insulate said second contact stud from said interconnect line; and

forming a conductive plug electrically connected to said second contact stud and within said insulating sidewalls.

38. The method of claim 37, wherein said first and second contact studs are formed simultaneously.

39. The method of claim 37, wherein the removed portion of said second contact stud is a silicide cap portion.

40. The method of claim 37, wherein said interconnect line is a bit line.

41. The method of claim 37, further comprising providing a capacitor in electrical contact with said second contact stud.

42. The method of claim 41, comprising forming a bottom electrode of said capacitor simultaneously with the forming of said conductive plug.

43. The method of claim 37, comprising forming said conductive plug by selective deposition of epitaxial silicon.

44. The method of claim 37, wherein said conductive plug is formed of a material selected from the group consisting of polysilicon and a metal-based material.

45. The method of claim 44, wherein said metal-based material is formed of one or more materials selected from the group consisting of W, TiN, Pt, Ru, and Al.

46. The method of claim 44, wherein said metal-based material is formed of one or more materials selected from the group consisting of a metal selected from Groups IVB, VB, VIB, VIII, IB, IIB, or IIIA of the Periodic Table, alloys of the preceding, oxides of the preceding, carbides of the preceding, borides of the preceding, and combinations of the foregoing

47. A memory device, comprising:

a first conductive silicon-containing stud and a second conductive silicon-containing stud;

an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive silicon-containing stud; and

an insulating material separating said interconnect line from said second conductive silicon-containing stud.

48. The memory device of claim 47, wherein said first and second conductive silicon-containing studs are epitaxial silicon.

49. The memory device of claim 48, wherein said first conductive epitaxial silicon stud has a silicide cap and said second conductive epitaxial silicon stud does not have a silicide cap.

50. The memory device of claim 48, wherein said interconnect line is a bit line.

51. The memory device of claim 48, wherein said insulating material extends to provide insulating sidewalls within a contact opening to said second conductive epitaxial silicon stud, wherein said contact opening is through an insulating layer which is over and around said interconnect line.

52. The memory device of claim 51, comprising a conductive plug to said second conductive epitaxial silicon stud within said insulating sidewalls.

53. The memory device of claim 52, wherein said conductive plug forms a capacitor bottom electrode.

54. The memory device of claim 48, wherein said first and second conductive epitaxial silicon studs are connected to respective source and drain regions of a transistor.

55. The memory device of claim 54, wherein said first conductive epitaxial silicon stud is between wordline gates and said second conductive epitaxial silicon stud is between a wordline gate and an isolation gate.

56. The memory device of claim 54, wherein said transistor is an access transistor of a memory cell.

57. The memory device of claim 50, wherein said conductive plug comprises epitaxial silicon.

58. A DRAM cell structure, comprising:

an access transistor with source and drain areas;

a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud each in contact with a respective one of said source and drain areas of said access transistor;

a bit line over and in electrical contact with said first conductive epitaxial silcon stud, wherein at least a portion of said bit line overlays a portion of said second conductive epitaxial silicon stud; and

an insulating material separating said bit line from said second conductive epitaxial silicon stud.

59. The DRAM cell structure of claim 58, wherein said first conductive epitaxial silicon stud has a silicide cap and said second conductive epitaxial silicon stud does not have a silicide cap.

60. The DRAM cell structure of claim 58, wherein said insulating material is an insulating sidewall within a contact opening to said second conductive epitaxial silicon stud, wherein said contact opening extends through an insulating layer over and around said bit line.

61. The DRAM cell structure of claim 60, comprising a conductive plug within said insulating sidewall and in contact with said second conductive epitaxial silicon stud.

62. The memory device of claim 61, wherein said conductive plug is a capacitor bottom electrode.

63. The DRAM cell structure of claim 61, wherein said conductive plug is epitaxial silicon.

64. A DRAM cell structure, comprising:

at least one wordline gate and at least one isolation gate on a semiconductor substrate;

an insulating layer on and around said at least one wordline gate and said at least one isolation gate;

at least one first epitaxial silicon stud with a silicide cap and at least one second epitaxial silicon stud without a silicide cap, each said stud in contact with a respective source and drain region of said at least one wordline gate;

at least one bit line over and in electrical contact with said at least one first epitaxial silicon stud and partially overlying said at least one second epitaxial silicon stud, but electrically isolated therefrom by an insulating sidewall; and

a conductive plug within said insulating sidewall and in electrical contact with said second epitaxial silicon stud.

65. The DRAM cell structure of claim 64, wherein said first epitaxial silicon stud is between said at least one wordline gate and a second wordline gate, and said second eptiaxial silicon stud is between said at least one wordline gate and said at least one isolation gate.

66. The DRAM cell structure of claim 64, wherein said second epitaxial silicon stud is a capacitor stud.

67. The DRAM cell structure of claim 64, wherein said conductive plug forms a capacitor bottom electrode.

68. The DRAM cell structure of claim 64, wherein said conductive plug is epitaxial silicon.

69. A processor-based system, comprising:

a processor; and

a memory circuit connected to said processor, wherein said memory circuit includes a memory device comprising:

a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud;

an interconnect line over and in electrical contact with said first conductive stud, wherein a portion of said interconnect line overlays a portion of said second conductive epitaxial silicon stud; and

an insulating material separating said interconnect line from said second conductive epitaxial silicon stud.

70. The processor-based system of claim 69, wherein said first conductive epitaxial silicon stud has a silicide cap and said second conductive epitaxial silicon stud does not have a silicide cap.

71. The processor-based system of claim 69, wherein said interconnect line is a bit line.

72. The processor-based system of claim 69, wherein said insulating material extends to provide insulating sidewalls within a contact opening to said second conductive epitaxial silicon stud, wherein said contact opening is through an insulating layer which is over and around said interconnect line.

73. The processor-based system of claim 72, comprising a conductive plug to said second conductive epitaxial silicon stud within said insulating sidewalls.

74. The processor-based system of claim 73, wherein said conductive plug forms a capacitor bottom electrode.

75. The processor-based system of claim 71, wherein said first and second conductive epitaxial silicon studs are connected to respective source and drain regions of a transistor.

76. The processor-based system of claim 75, wherein said first conductive epitaxial silicon stud is between wordline gates and said second conductive epitaxial silicon stud is between a wordline gate and an isolation gate.

77. The processor-based system of claim 75, wherein said transistor is an access transistor of a memory cell.

78. The processor-based system of claim 73, wherein said conductive plug comprises epitaxial silicon.